

SYNPLIFY PREMIER

The Ultimate FPGA Implementation Platform

The Best of Both Worlds: Productivity & Performance

- ▶ Best Quality of Results for Timing Performance and Area/Cost Reduction
- ▶ Automated Multiprocessing, Fast Synthesis and Incremental Flows for Fast Turnaround Time
- ▶ Broad Language Support for Verilog, VHDL, VHDL2008 and SystemVerilog
- ▶ Debug of an operating FPGA, directly in RTL code
- ▶ Safety Critical Features such as Safe FSM and TMR for High Reliability Applications
- ▶ Early Power Analysis and Optimization
- ▶ FPGA-Based Prototyping Including DesignWare® IP Support

“The Telecommunications market demands the most advanced and complex ICs in short intervals. We rely on Synopsys’ Synplify Premier product for prototyping ASIC designs on large Altera and Xilinx devices.”

Mehmet Ekmen
Team Leader, ST Ericsson

Overview

Trends point to an increase in use of programmable chips thanks to the relentless rise in capacity, making FPGA design a top growth segment in the semiconductor industry. However, these same trends mean that designers are now experiencing some tough new challenges. For example, FPGAs at 28nm have the equivalent capacity of a twenty million ASIC gate design. These types of advanced FPGA designs need tools and methodologies that deliver automation, faster turnaround times, more predictable timing closure, high reliability, power management, advanced verification techniques and the integration of IP. The tool best equipped to handle these design challenges is the Synplify® Premier implementation and debug software from Synopsys. This software platform automates many functions so that designers can focus on their own product differentiation while meeting schedule and cost targets.

The Best Quality of Results

If design performance is not achieved, then nothing else really matters. The Synplify Premier tool uses state of the art timing-driven synthesis technology to first and foremost meet timing. Once met, it focuses on logic reduction to fit in the smallest, least expensive FPGA possible. Enhanced Synthesis Mode is a feature unique to Synplify Premier where additional advanced optimizations are used to maximize timing performance. Enhanced mode uses the same design constraints used for normal logic synthesis making it very easy to apply.

Fast Design Turnaround Times

Synplify Premier is the fastest FPGA synthesis tool available and with the addition of two new techniques synthesis runtimes can be reduced up to 10X compared to normal logic synthesis.

Hierarchical—As FPGA designs grow in size and complexity, it has become common that teams of designers and parallel development techniques are used to ensure large projects are more easily managed and finished on schedule. The hierarchical design features in Synplify Premier enable designs to be split into smaller sub-projects with different engineers or teams working on each sub-project independently. Sub-projects are self-contained, enabling remote development and reuse of blocks on future projects. The hierarchical design feature in the Synplify Premier product supports both top-down and bottom-up methodologies.

Fast mode—The Synplify Premier software’s fast synthesis mode was created to get a design on the board quickly for fast initial analysis. Designers are seeing 3x faster turnaround time for implementation of FPGAs when using fast mode. This allows system software development and porting to begin and the working system to be assessed, updated and verified without delay.

Multiprocessing with Compile Point RTL Partitions—Combining multiprocessing and fast mode together, designers can achieve up to a 10X logic synthesis runtime speedup with some small loss in QoR. Compile Points are RTL partitions that can be created either manually or automatically by the tool and are used to partition a design for multi-processing.

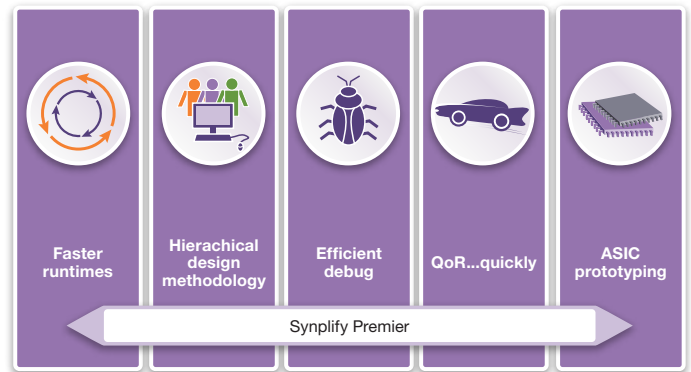


Figure 1: Synplify Premier

Incremental—Synplify Premier supports incremental design techniques, such as Xilinx’s SmartGuide, and Design Preservation flows as well as Altera’s partition flow which can greatly reduce turnaround time from RTL to board. Additionally, Compile Points and FPGA vendor P&R tools together deliver a fully integrated incremental flow eliminating the need to re-synthesize and re-verify unchanged portions of the design. Designers can then focus on refining targeted blocks or critical paths by isolating them within a Compile Point.

Broad RTL Language Support

Taking advantage of the latest HDL developments such as SystemVerilog and VHDL2008 provides an advantage in engineering productivity. Less time spent coding RTL means more time for design architecture exploration and developing product differentiation. Mixed language support has become the

“We were very impressed with Synplify Pro’s ability to meet all targets—area, performance and timing – on the first try. We succeeded in reducing both risk and cost for multiple designs.”

Dhiraj Mallick
VP of Hardware and System Engineering, SeaMicro

“Some of the bugs that come up in real life today require that we monitor a thousand signals or more at the same time. Thanks to the Identify tool, we’re able to tackle and fix these complex bugs.”

Sandesh Bharadwaj
Staff Engineer, MIPS Technologies

standard for many FPGA designers as IP from various sources is incorporated into today’s designs. For FPGA prototypers the Synplify Premier tool’s language support encompasses VHDL, VHDL2008, SystemVerilog, and Verilog and is compatible with Synopsys’ Design Compiler ASIC synthesis products. Advanced features such as Verilog Cross Module References are provided. System Verilog Assertions are parsed and ignored, allowing designers to synthesize and verify designs from the RTL source.

Debug Where You Design, In RTL

The Identify RTL Debugger is integrated into the Synplify Premier software, allowing designers to debug and validate FPGAs running on the board, relating design operation directly back to their RTL code. Designers can easily define watch points and sophisticated trigger conditions, perform highly customizable sampling and generate data for a waveform viewer display. Qualified sampling that is highly customizable allows users to pinpoint exact data signals and operating conditions of interest. Using Identify for the RTL-Level debug of FPGAs is intuitive and results in improved product quality.

Safety Critical Features

Synplify Premier includes features to support high reliability applications such as medical and the harsh environments of industrial automation, military and aerospace. These high reliability capabilities are useful for implementing DO-254 compliance and include:

- ▶ Safe Finite State Machines (FSMs) implementation options
- ▶ Triple Module Redundancy (TMR) with voting logic
- ▶ Controls that limit synthesis optimizations allowing designers to maintain critical logic and nodes within the design for verification, equivalence checking, requirements traceability, or monitoring of the design operation in the field
- ▶ Highly customizable design reporting using TCL/FIND and HDL Analyst
- ▶ Design Analysis at the RTL and netlist level using HDL Analyst
- ▶ FPGA debug on the board using the Identify RTL Debugger
- ▶ Repeatable synthesis results and netlist naming conventions from one synthesis run to the next

Power Analysis and Optimization

The Synplify Premier software includes advanced techniques for power reduction. With the flip of a switch the tool automatically generates high quality switching activity data in SAIF format that may be used for power analysis and reporting or to drive power reduction optimizations. With this switching activity data users can now get an early power estimate pre-P&R and adjust their RTL accordingly without the need for creating a simulation testbench. The Synplify Premier tool also has the ability to turn off unused bits in RAM and DSP blocks when directed to reduce dynamic power consumption.

FPGA-based Prototyping Support

The Synplify Premier software uniquely delivers RTL compatibility between FPGA and ASIC flows allowing designers to synthesize the same ASIC RTL source files into an FPGA. Complete integration is provided for all digital IP in the DesignWare Library meaning that the DesignWare components used in ASIC and FPGA flows are completely synchronized, ensuring flow compatibility and accurate verification.

For ASIC prototyping, designers use Synopsys’ FPGA-based prototyping solution which includes both HAPS® hardware and a comprehensive software environment based on Synplify Premier synthesis technology. This integrated hardware plus software solution enables pre-silicon software development and hardware/software co-verification of both subsystems and complete systems at near real-time speeds using real-world interfaces.

“Other tools can’t handle the complex constructs of the ASICs we’re working on. Only Synplify Premier gives us the ability to synthesize native ASIC code untouched for our FPGA prototype.”

David Garau
Engineering Manager, Silicon Validation Group, Teradici

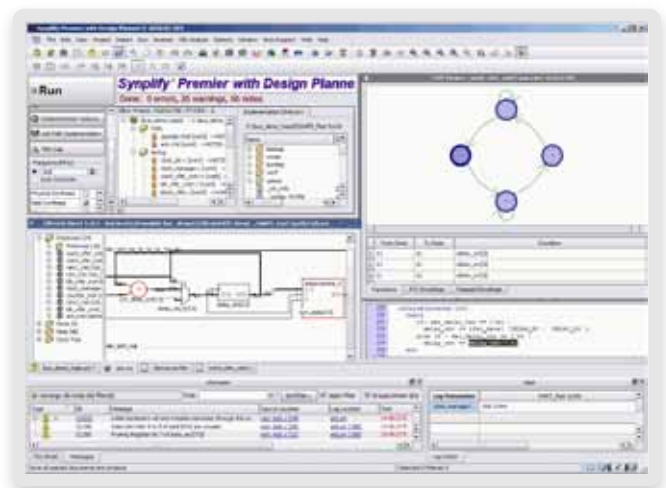


Figure 2: Synplify Premier

At-a-Glance: Synplify Premier Advanced FPGA Design Capabilities

Feature	Benefits
All of Synplify Pro, Plus	<ul style="list-style-type: none"> • Run either Synplify Pro or Synplify Premier with a Synplify Premier license • Support for the latest VHDL and Verilog language constructs including SystemVerilog and VHDL 2008 • Support for a variety of FPGA vendors including Altera, Lattice, Microsemi (formerly Actel), SiliconBlue and Xilinx • Integrated HDL Analyst for fast isolation of critical paths and RTL code analysis
Fast Synthesis Mode	<ul style="list-style-type: none"> • Up to 4X synthesis speedup with tight timing constraints • Up to 3X RTL to bit-file speedup with loose timing constraints • Quickly create a working chip implementation on a board • Fast feedback on RTL and constraints to quickly tune the design
Multiprocessing with Compile Points	<ul style="list-style-type: none"> • Partition design manually or automatically to synthesize in parallel using multiple processor cores • Use with normal logic synthesis to achieve up to a 3X synthesis speedup • Use together with Fast Mode for up to 10X synthesis speedup
Enhanced Synthesis	<ul style="list-style-type: none"> • Improve timing results at the flip of a switch, with additional logic synthesis optimizations including the ability to optimize inside Xilinx IP
Integrated RTL Debugger	<ul style="list-style-type: none"> • Faster and higher quality debug at the RTL-Level (vs. gate-level) • Quickly create higher quality, more fully verified FPGA designs • Easily define watch points and sophisticated trigger conditions automatic compilation and insertion of debug logic into the RTL and FPGA implementation
Power Optimizations	<ul style="list-style-type: none"> • Pre-P&R power estimates allow early optimization of RTL for power • Generate high quality switching data to drive power optimizations • Automated power conservation for unused RAM blocks • Automatic power optimization of Xilinx DSP48 primitives
DesignWare IP Integration	<ul style="list-style-type: none"> • Fully synchronized ASIC to FPGA flows for DesignWare components • The only FPGA synthesis tool to provide complete integration with DesignWare Library digital IP allowing high quality of results when re-targeting to FPGA any ASIC RTL source that contains DesignWare components
FPGA-Based Prototyping Support	<ul style="list-style-type: none"> • Easily re-target ASIC source code to FPGA-based prototypes • RTL debug of design operating on the board • HAPS prototyping board integration • Netlist Editor and Compiler Constraints Feature streamlines-import and retargeting of ASIC code for an FPGA

Ask your sales representative about evaluating Synplify Premier,
or find more information at: www.synopsys.com/synplifypremier.



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