TSV Stress Management

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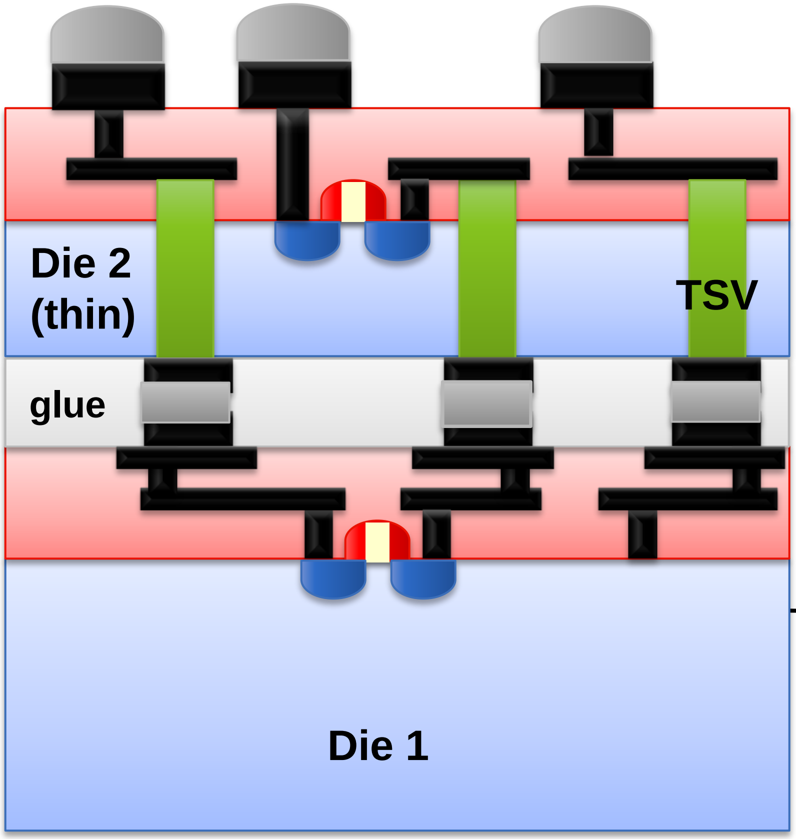
DATE 2010

Outline

- TSV related performance and reliability issues due to thermal-mechanical stress
- Fammos capability overview
- Modeling TSV stress and related effects using Fammos
- Summary
- Questions and answers

TSV Related Performance and Reliability Issues

Typical Back-to-Front TSV Stack



Bumps to connect to the package

Interconnects

TSV: Through Silicon Via

Micro-bumps

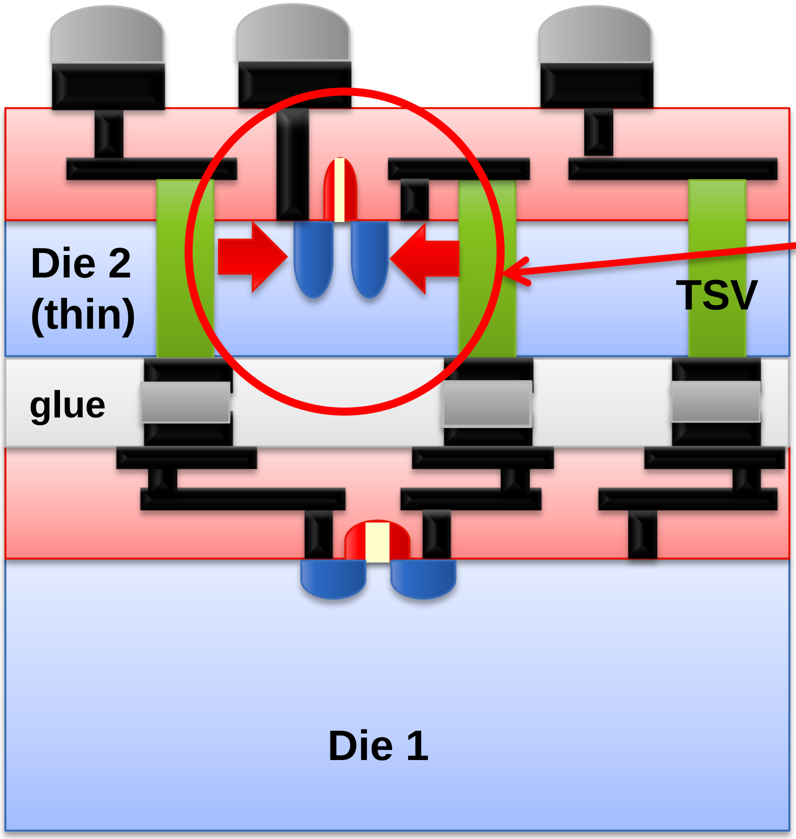
Interconnects

Transistors

Thermal Mismatch
Silicon CTE: 3.05 ppm
Copper CTE: 17.7 ppm

New stress from materials in TSV stack

TSV Induced Proximity Effects



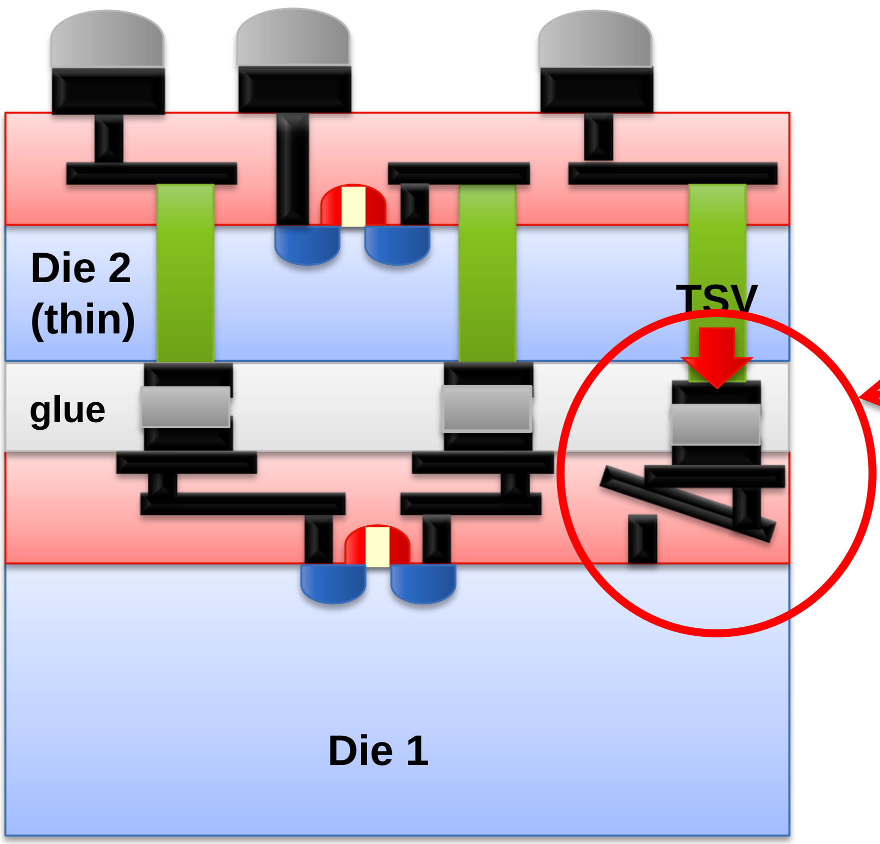
Transistor is being squeezed or stretched by adjacent TSVs

Material deformation leads to mobility change

The amount of proximity effects depend on geometry shape, location, and orientation

Stress affects transistor performance

TSV Related Reliability Concerns



TSV squeezes or stretches adjacent interconnects

De-bonding and De-lamination could occur under additional stress

Stress affects BEOL reliability

Modeling Requirements

- **Stress sources**
  - Intrinsic bonding from material formation
  - Lattice mismatch from crystal growth
  - Thermal expansion mismatch from process flow
  - External loading from stacking and packaging
- **Structure generation & stress evolution**
  - Fabrication process: deposition, etching
  - Layout from design specs
- **Models for stress effect**
  - Stress-to-electrical models for performance
  - Stress-to-damage models for reliability

Fammos Capability Overview

Fammos TX Highlights

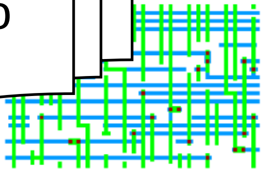
- **3D Structure Generation**
  - Process steps
  - Mask layouts (GDSII)
- **Detailed Process Steps**
  - Deposition:
    - Isotropic, anisotropic, planar, patterned, tapered
  - Etching:
    - Isotropic, anisotropic, planar, tapered
- **Multiple Stress Sources**
  - Intrinsic, grain growth, thermal mismatch, applied
- **Models**
  - BEOL reliability
  - Silicon mobility variation

Fammos TX 3D Simulation Flow

Deposition
Etch mask=

Process Info

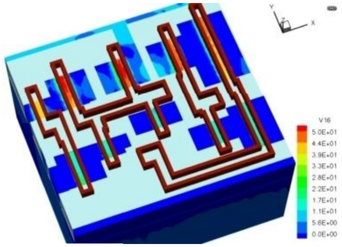
Layout Info
(GDSII)

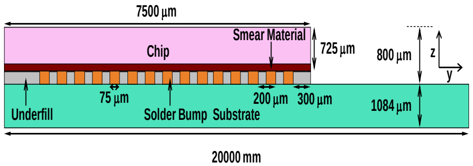


Material Property
Database

Fammos TX

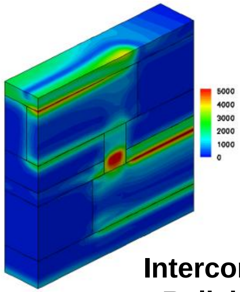
Mobility Variation



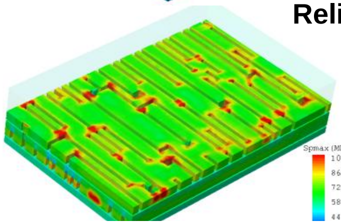


Packaging Reliability

3D Structure
Stress Field
Reliability
Mobility Variation

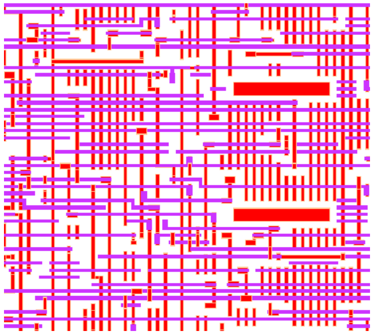


Interconnect Reliability



Stress Hotspot

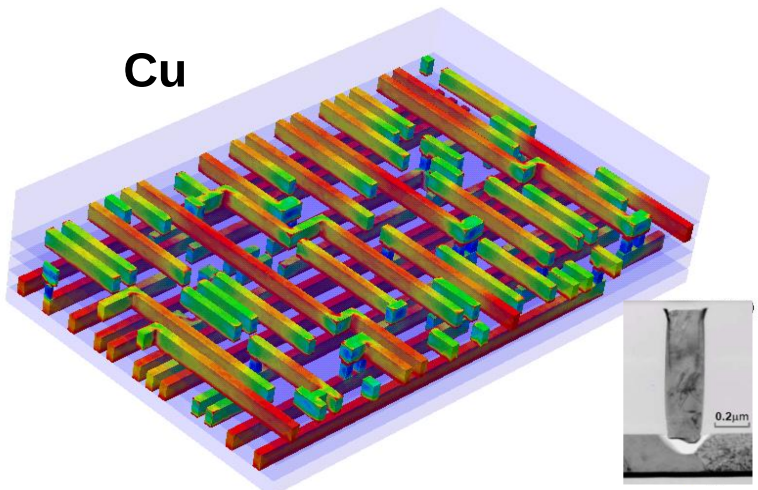
Example: 3D Simulation from Layout



Layout

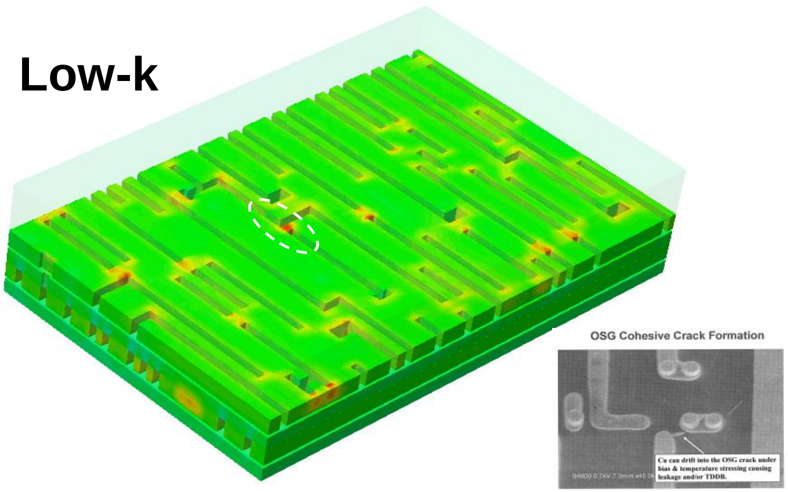
```
# Import GDS layout
STRUCTURE maskfile=my.gds block=cell2

# Identify mask layers
ASSIGN name=metal2 index=2
ASSIGN name=metal3 index=3

# Define simulation domain size
DOMAIN xmin=10 xmax=19 ymin=10 ymax=16
```

Cu



Cu Lines at Metal 2&3 in a 9um x 6um Window in a 90nm Chip

Low-k

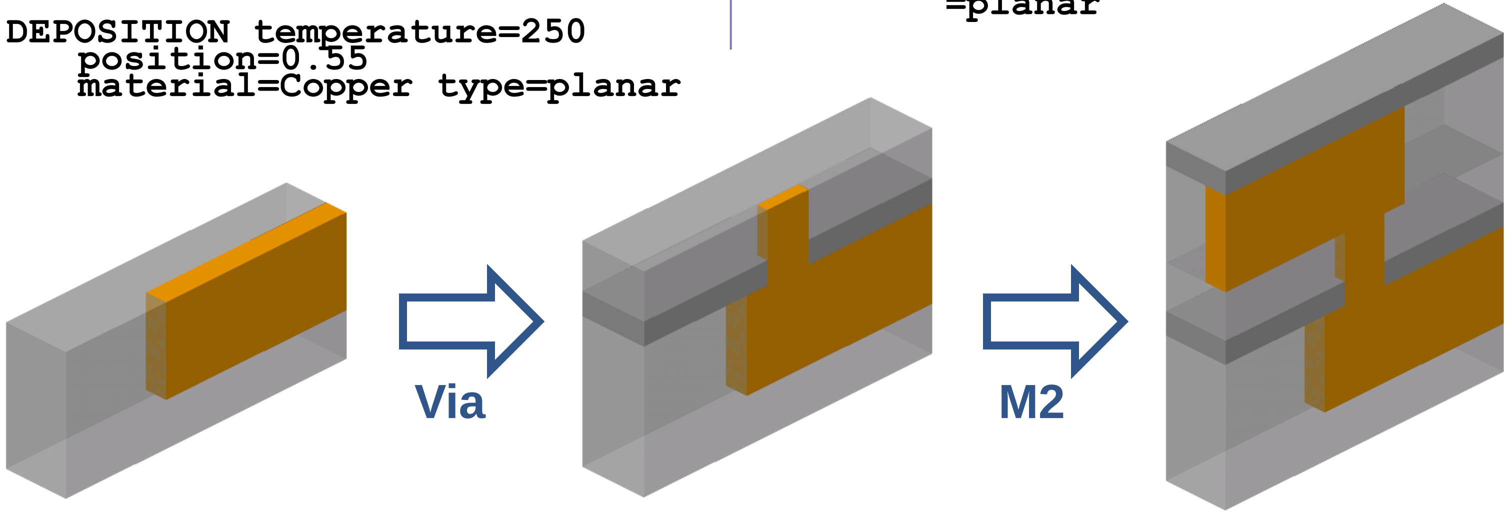


High stress hotspot in low k dielectrics

Example: Deposit, Etch, Thermal Cycling

```
DEPOSITION temperature=250
    position=0.45
    material=Nitride type=planar

DEPOSITION temperature=250
    thickness=0.1 material=Low-k
    type=isotropic

ETCH temperature=25
    material=Low-k mask=via12
    thickness=0.1 negative
    type=isotropic

ETCH temperature=25
    material=Nitride mask=via12
    thickness=0.05 negative
    type=isotropic

DEPOSITION temperature=250
    position=0.55
    material=Copper type=planar
```

```
DEPOSITION temperature=250
    thickness=0.2 material=Low-k
    type=isotropic

ETCH temperature=25
    material=Low-k mask=metal2
    thickness=0.2 negative
    type=isotropic

DEPOSITION temperature=250
    position=0.75 material=Copper
    type=planar

DEPOSITION temperature=250
        tion=0.8 material=Nitride
        =planar
```

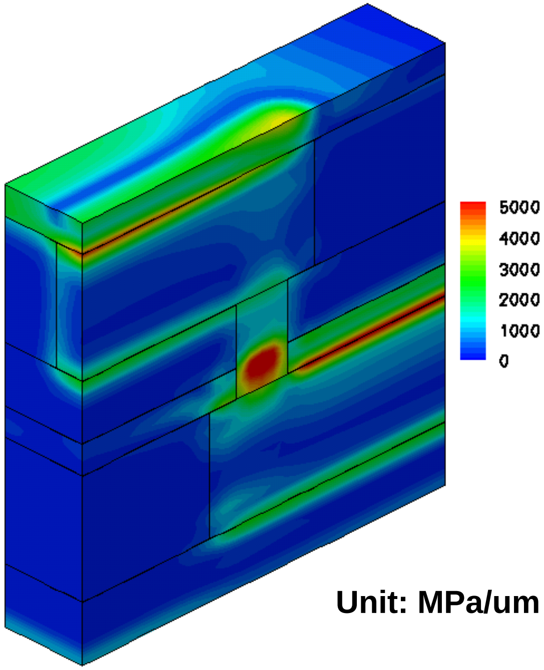


Stress Migration Model for Metal Voiding

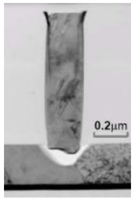
- **Stress driven vacancy diffusion** (TSMC scheme)

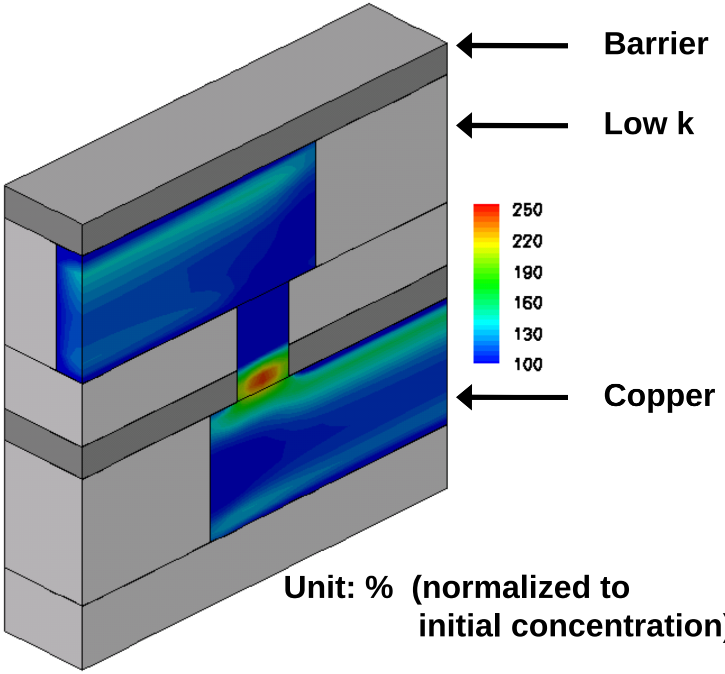
$$\nabla^2 C = \frac{1}{D}\frac{\partial C}{\partial t} - \frac{1}{kT}\nabla \cdot \nabla \sigma_H$$

T.C. Huang, *et al.*, IITC 2003



Hydrostatic stress gradient magnitude



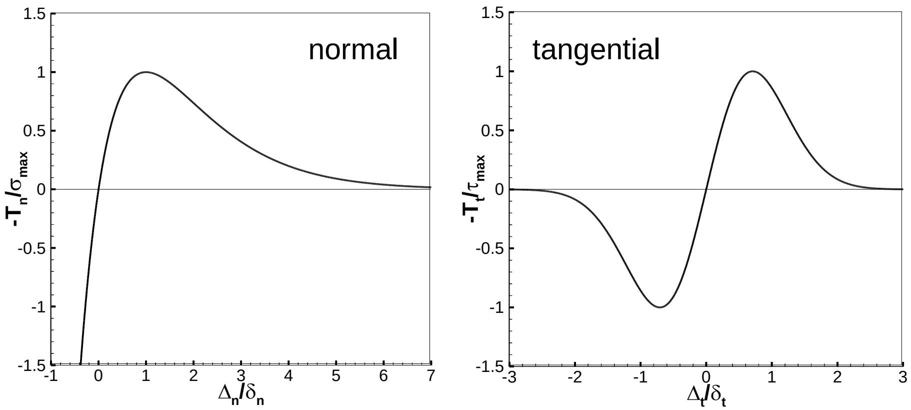


Accumulated vacancy density in metal

Fammos simulation Results

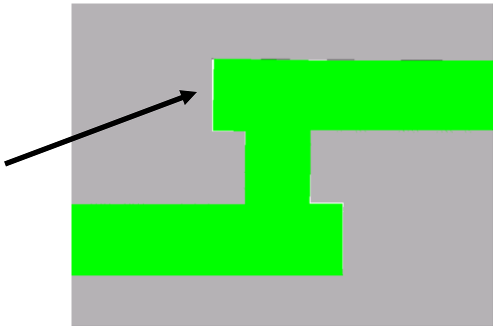
Interface De-bonding Simulations

Cohesive zone model

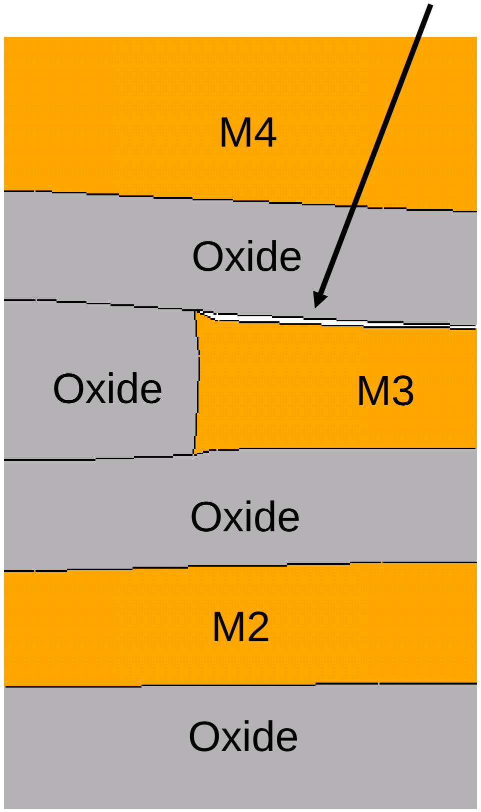


X. Xu and A. Needleman, 1994, JMPS

De-bonding

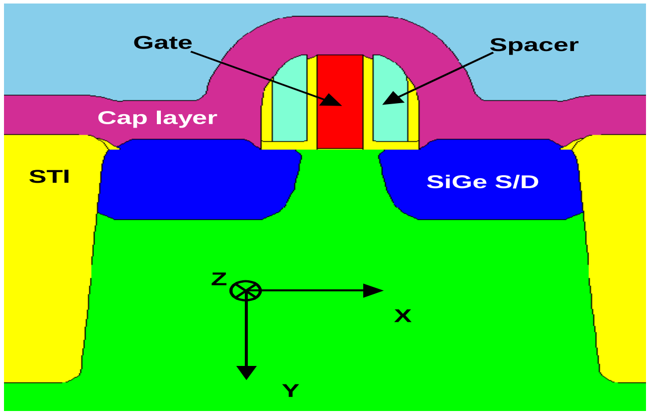


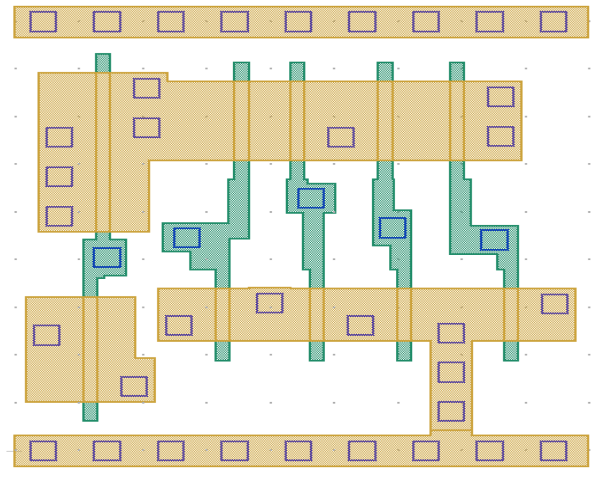
De-lamination

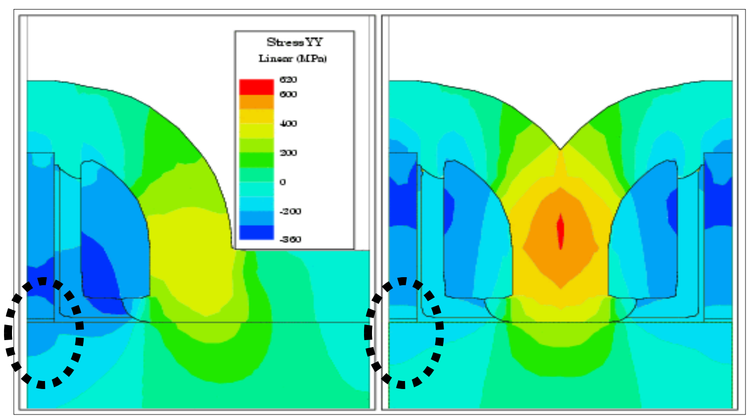


Large stress and weak interface leads to de-bonding

Stress and Mobility Variation in Layout

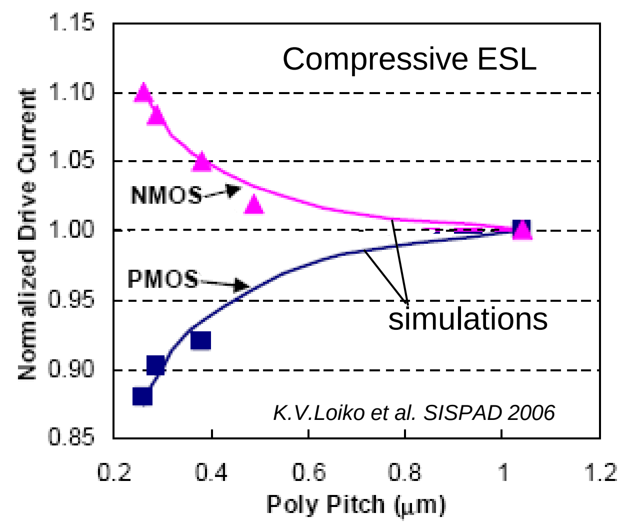




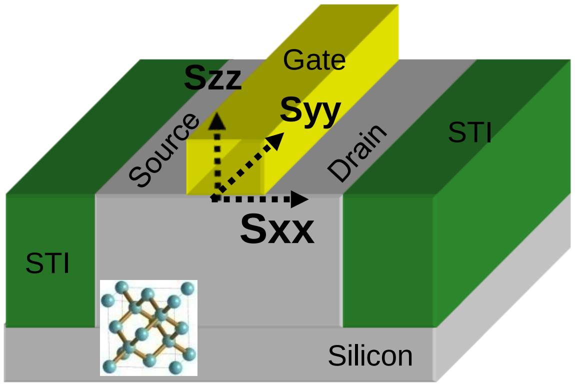


320nm pitch

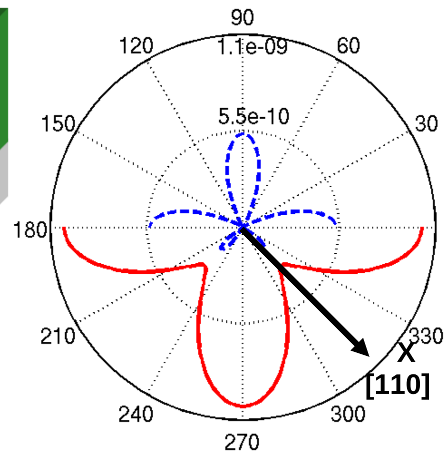
160nm pitch



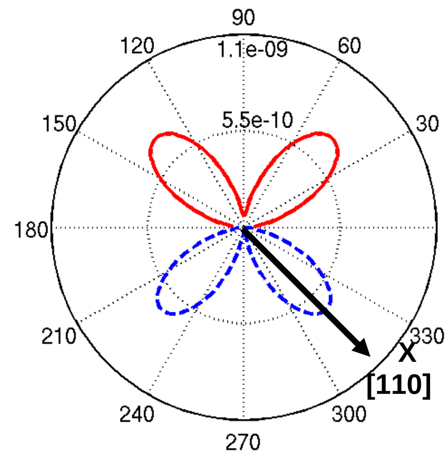
Piezo Converts Stress Into Mobility

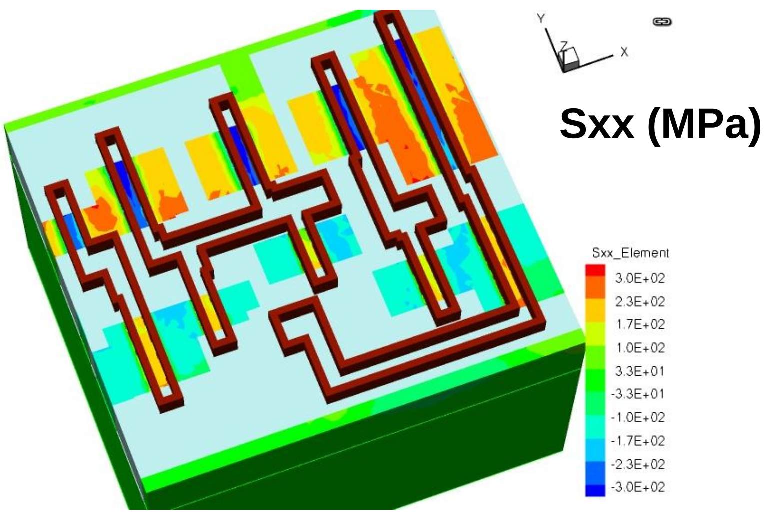


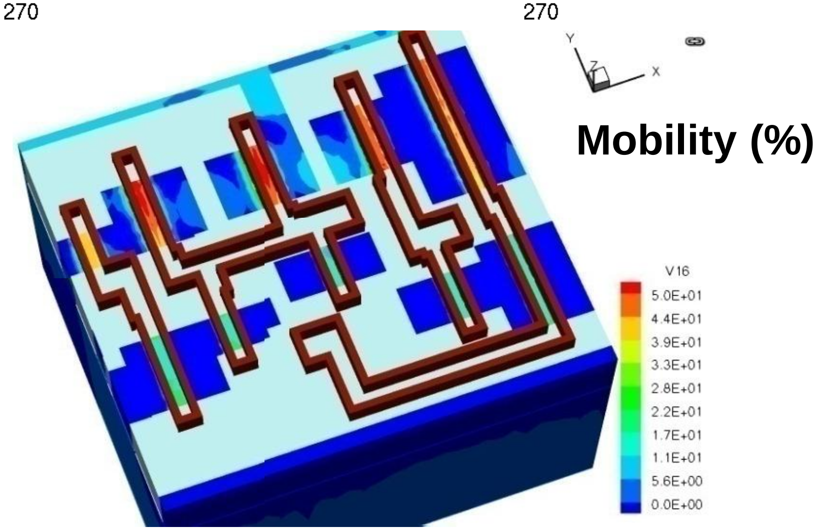
001 Wafer n-Si



001 Wafer p-Si

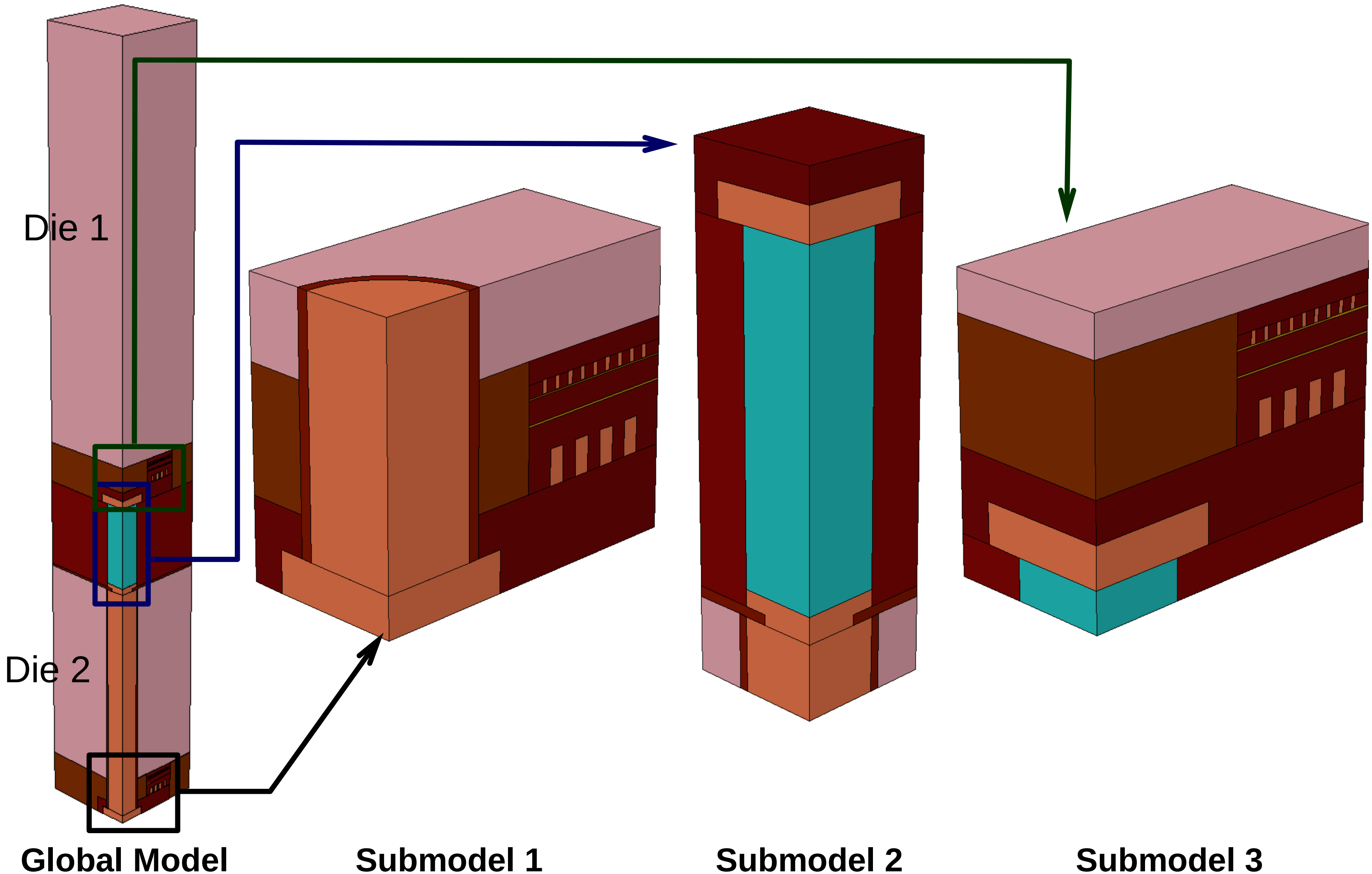






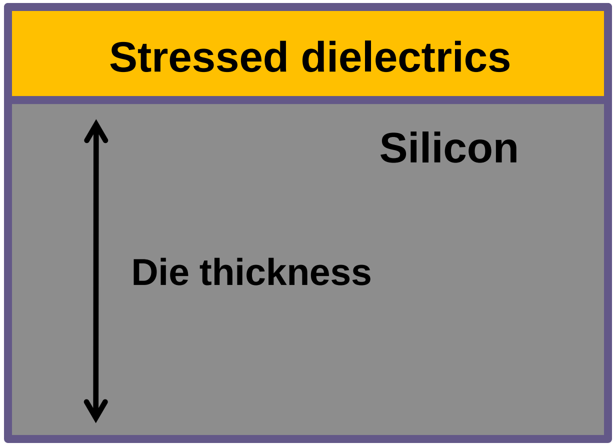
Modeling TSV Induced Effects with Fammos

Multi-scale Modeling with Global and Sub-models

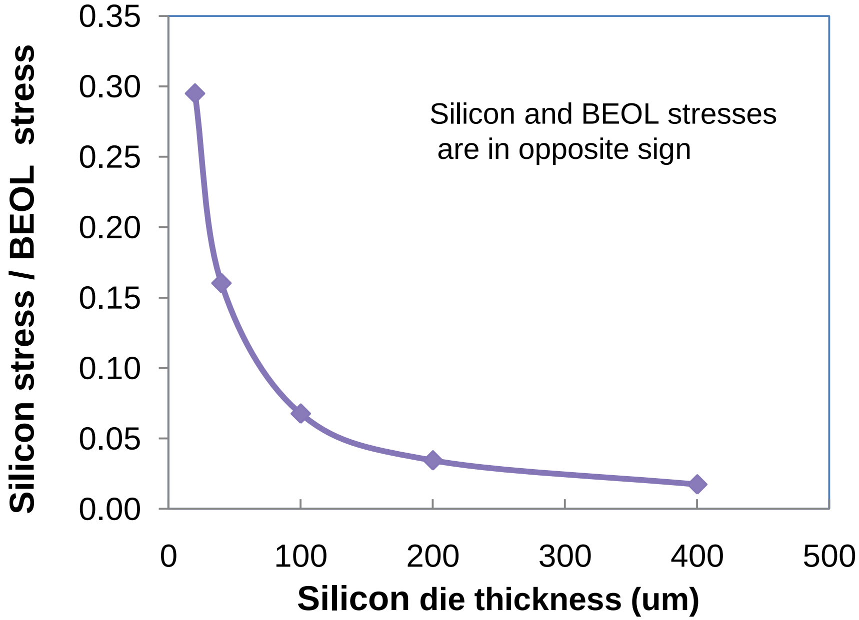


Effect of Die Thinning

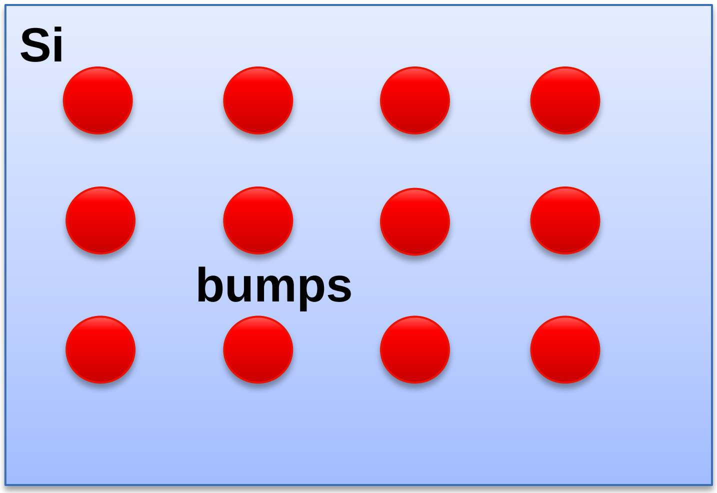
- Interconnect/dielectrics layers are under thermal mismatch stress
- Stress transfers from dielectric layer to active silicon due to die thinning
- Transferred stress depends on thickness



Cross-section segment

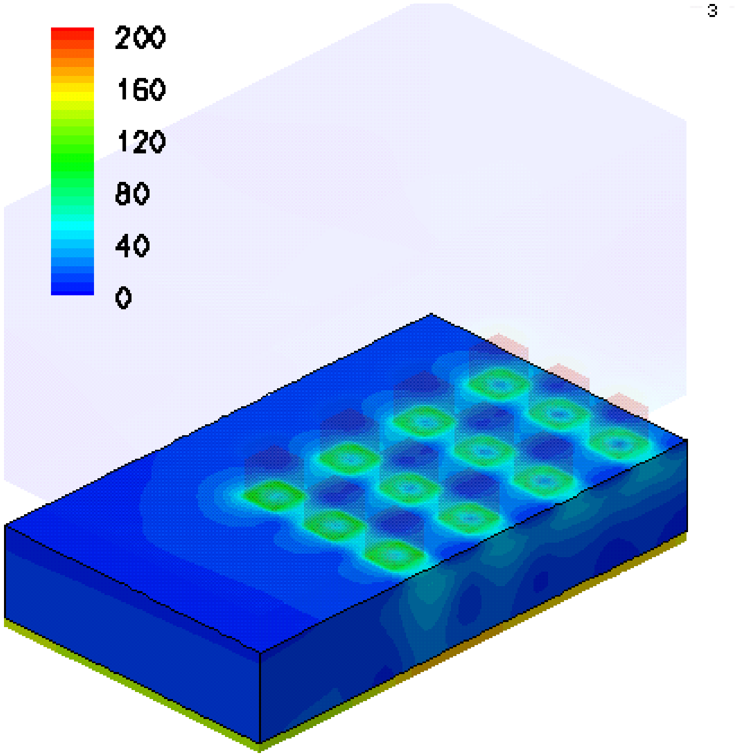


Stress Distribution Around μ-bumps



Top View of u-bumps Between Dies

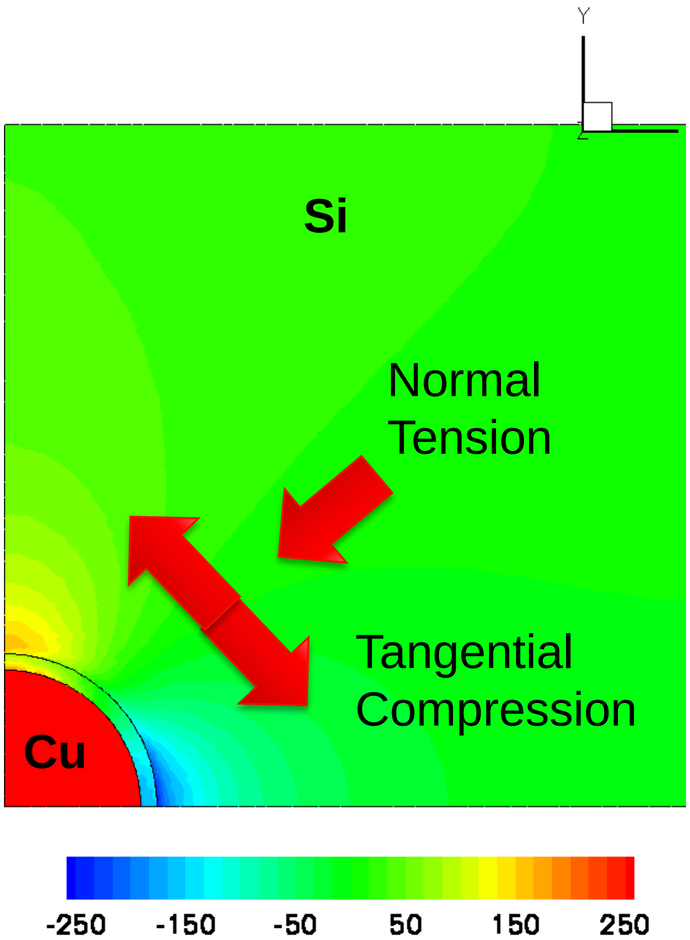
Von Mises Effective Stress in Mega Pascal



High stress levels around μ-bumps

SYNOPSYS® Predictable Success

Stress Distribution on Silicon Surface

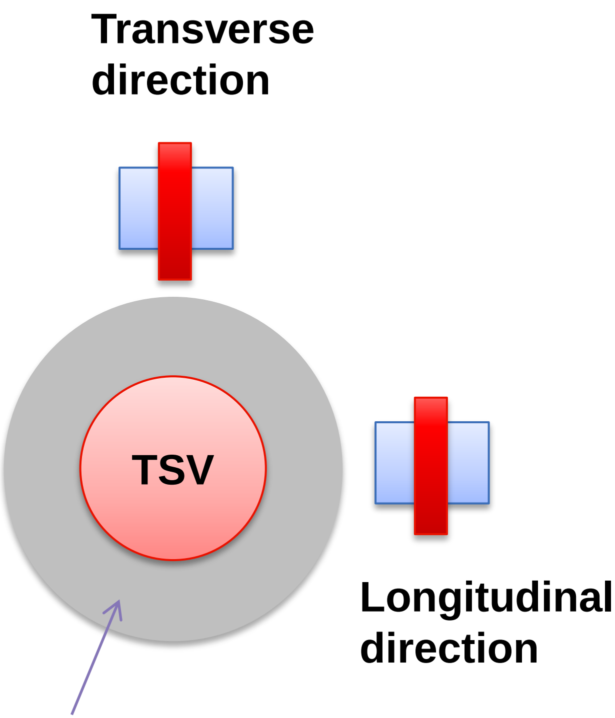


S_{yy} **Stress Component (MPa)**

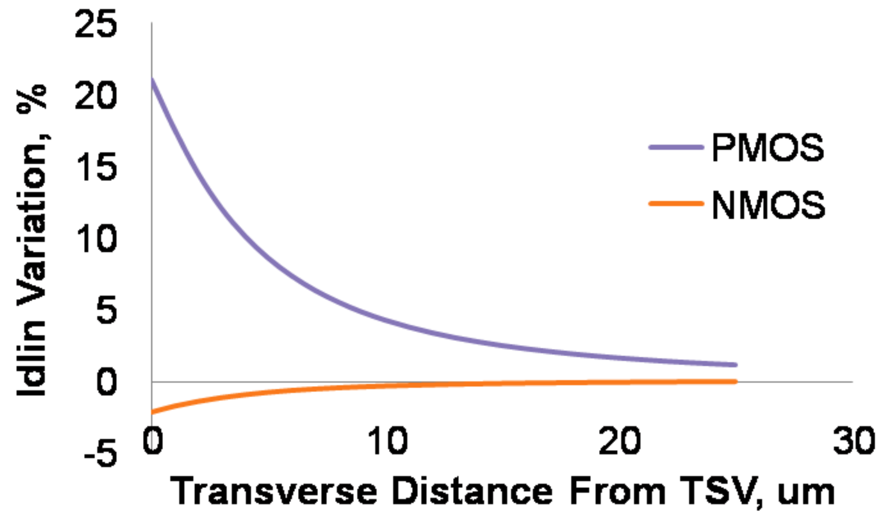
- **Copper filling of TSV happens at high temperature**
- **Upon cooling, Cu shrinks more than Si**
- **This leads to normal tension and tangential compression**
- **The range of stress propagation depends on TSV size, and typically is ~20μm**

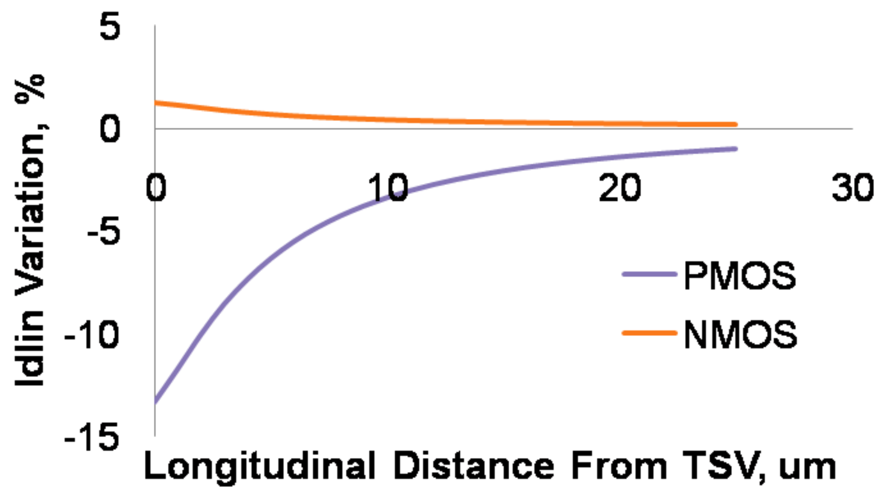
SYNOPSYS®
Predictable Success

Keep-Out Area Around TSVs

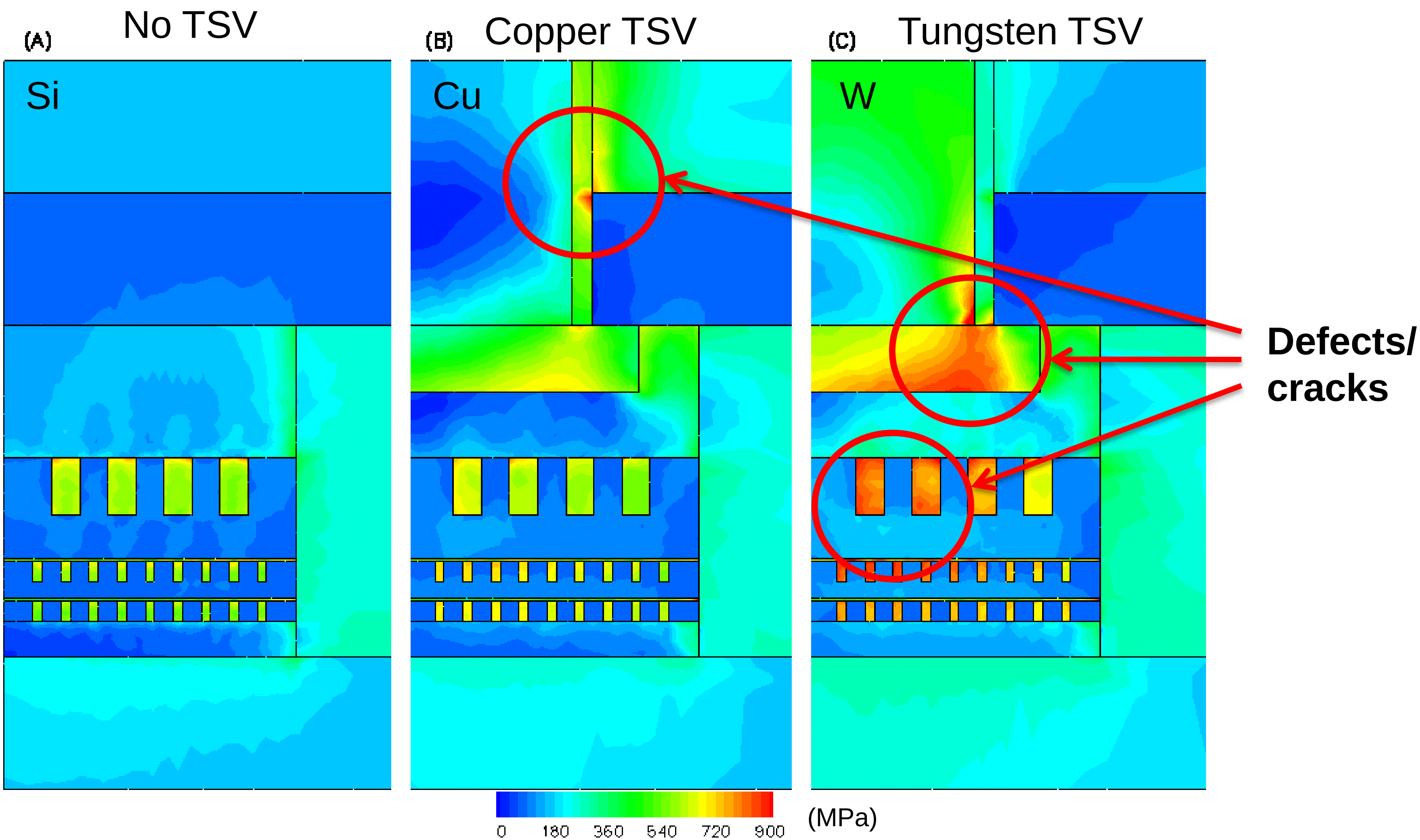


Keep-Out Zone
~10um for digital circuits, and
~20um for analog circuits





Reliability Impact – Effective Stress



Summary

- TSV introduces new stresses which affect performance and reliability
- Synopsys' Fammos TX is a state-of-the art process and mechanical stress simulator for semiconductor applications
- Multi scale process and stress simulations have been performed using Fammos to analyze TSV impact on performance and reliability